



TITLE OF THE INVENTION

VARIABLE GAIN AMPLIFIER, SOLID-STATE IMAGING DEVICE AND OPTICAL SIGNAL READING METHOD

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a variable gain amplifier capable of adjusting a gain according to a level of an input signal, to a solid-state imaging device for converting an optical signal into a digital signal and outputting the digital signal, which is used for a video camera, an electronic camera, an image input camera, a scanner, a facsimile or the like, and to an optical signal reading method.

15 2. Description of the Related Art

A semiconductor image sensors such as a CCD image sensor and a MOS image sensor are excellent in mass production, and thus such sensors have been applied to many image input devices along with an advance in a fine patterning technology.

Especially, in recent years, a CMOS image sensor has been a main focus of attention because of its advantages in contrast with the CCD image sensor, i.e., smaller power consumption, and capability of fabricating a sensor device and a peripheral circuit device by the same CMOS technology.

Such a CMOS image sensor is described in US Patent

No. 6,128,039. The CMOS image sensor disclosed in US Patent No. 6,128,039 is called an active pixel sensor. As shown in Fig. 1 transferred from this US patent, in combination with an active load such as a constant current source M4 or the like, a signal voltage is outputted by a source follower.

In the CMOS image sensor of US Patent No. 6,128,039, a load capacitor C1 for storing signal charges and a gate-source capacitor Cgs of the reading transistor M2 are connected in series to a gate of M2. These capacitors are set parallel in a fixed capacitor for charge/voltage conversion, and the fixed capacitor for charge/voltage conversion is seemingly changed in the capacitance. Charging of the capacitor C1 connected to the source of M2 greatly changes a source potential during signal reading. As this potential change is returned through the capacitor Cgs to the gate, an input potential is also changed, causing a considerable deterioration of linearity of a transmission characteristic. Consequently, in this CMOS image sensor, the constant current source M4 as a load of a reading transistor M2 was inevitable.

In addition, in recent years, a column type analog/digital converter of an integration system (hereinafter referred to as a column type ADC) has been mounted on the image sensor. In such a column type ADC, an analog electric signal (photoelectric signal) into

which an optical signal is converted is compared with a comparison lamp voltage having a predetermined gradient by a comparator, and is converted into a pulse count corresponding to an amplitude of the photoelectric signal by a pulse counter.

In such a case, when the analog signal is small, a gradient of the comparison lamp voltage is also reduced to secure a dynamic range.

Furthermore, in a solid-state imaging device including a number of unit pixels arrayed in horizontal and vertical directions, sampling pixels are thinned to output only detecting signals of remaining pixels not thinned during moving image reproduction, thereby increasing a frame rate.

However, in the case of the image sensor including the constant current source M4 for each column, since there are variances in characteristics among the respective constant current sources M4, variances are generated in gains among columns. This variance appears as an offset difference between columns, and when seen on a screen, the variance appears as a so-called vertical fixed pattern noise.

When a signal voltage outputted from the conventional image sensor is inputted to the column type ADC, a gradient of a comparison lamp voltage is reduced corresponding to a small analog signal. In this case, a limitation is placed on an S/N ratio because of linearity

of a lamp signal or comparison accuracy of the comparator, and because of an influence of an offset voltage generated in a photoelectric conversion device or the like.

5 Furthermore, if sampling pixels are thinned in the conventional image sensor, a modulation transfer function (MTF: resolution) is deteriorated, forming an image of much moire. In addition, when a reduction is made twice or lower as large as a sampling frequency proportional to
10 an inverse number of a sampling pixel interval because of the thinning of the sampling pixels, a folding noise (aliasing noise) may be thus generated. Also, as it is necessary to operate the image sensor at a high speed according to the number of pixels, power consumption is
15 increased.

SUMMARY OF THE INVENTION

This present invention is performed considering the foregoing drawbacks.

20 An object of the present invention is to provide a variable gain amplifier, a solid-state imaging device, and an optical signal reading method being capable of improving an S/N ratio while enhancing a dynamic range when a photoelectric signal is digitized.

25 Another object thereof is to provide a solid-state imaging device and an optical signal reading method being capable of reducing fixed pattern noises and further

suppressing a reduction in resolution and generation of folding noises while maintaining a low power consumption operation by thinning sampling pixels.

5 A variable gain amplifier of the present invention is characterized in that it converts a first signal voltage and a second signal voltage into charges by sequentially inputting the first and second signal voltages, generates a difference signal between the first and second signal voltages, amplifies the difference
10 signal by a gain so as to set the difference signal within a requested range of a digital encoding analog input level, and outputs the difference signal.

A variable gain amplifier comprises a so-called
15 chopper type switched capacitor integrating circuit. The chopper type switched capacitor integrating circuit includes, as shown in Fig. 2 as the example, an operational amplifier 31 having a positive input terminal (+) to which a reference voltage V_{ref} is applied and a negative input terminal (-), and an output terminal; an
20 input capacitor C_i (C_1) provided in a signal path extending from the input terminal of the variable gain amplifier 105a to the negative input terminal (-) of the operational amplifier 31; a feedback capacitor C_f composed of a plurality of capacitors (C_2 , C_3 ,
25 C_4 ,...etc.) provided between the negative input terminal (-) and output terminal of the operational amplifier 31; first switch devices SW1 and SW2 for

connecting/disconnecting a signal path extending from the input terminal of the variable gain amplifier 105a to the other end of the input capacitor C_i ; a second switch device SW3 for turning ON/OFF (connecting/disconnecting) an input of the reference voltage V_{ref} to the other end of the input capacitor C_i ; and a third switch device SW4 for connecting/ disconnecting a signal path between the negative input terminal (-) and output terminal of the operational amplifier 31.

An amplifying gain of the operational amplifier 31 can be adjusted as follows.

That is, the capacitors C_2 , C_3 , C_4 ...etc. constituting the feedback capacitor C_f are connected to switch devices (SW5, SW6...etc.) for controlling connection/disconnection of the respective capacitors between the input and output terminals of the operational amplifier 31. Accordingly, by selectively connecting/disconnecting the switch devices (SW5, SW6...etc.), a proper capacitor is selected and connected between the input and output terminals of the operational amplifier 31. Therefore, by increasing/reducing a capacitance of the feedback capacitor C_f , a ratio (C_i/C_f) of the input capacitor C_i with respect to the feedback capacitor C_f is adjusted. With this, it is possible to adjust the gain of the operational amplifier 31.

A solid-state imaging device comprises photoelectric conversion devices arrayed in rows and columns, the

foregoing variable gain amplifier provided for each of the columns and connected to outputs of the photoelectric conversion devices of each column, and an analog/digital conversion circuit for converting a difference signal into a digital signal, which is connected to an output side of the variable gain amplifier. In this case, a first signal voltage to be inputted to the variable gain amplifier is obtained by converting an optical signal into an electric signal, and a second signal voltage is obtained when the photoelectric conversion device is initialized.

The optical signal reading method is characterized in the followings. That is, the first signal voltage is converted into charges and then charges are stored, followed by outputting the second signal voltage and then converting it into charges. And the difference signal between the first signal voltage stored as charges and the second signal voltage converted into charges is amplified with the gain such that the difference signal is within the requested range of the digital encoding analog input level.

In other words, even when amplitude of the analog difference signal is smaller than the proper range of the digital encoding analog input level, the analog difference signal can be amplified to be properly set within the range of the digital encoding analog input level. As a result, when the analog difference signal is

digitized, it is possible to secure the dynamic range and to improve the S/N ratio.

Moreover, the foregoing solid-state imaging device includes the heavily doped buried layer for storing photo-generated charges (holes), which is provided below the channel of the MOS transistor for signal detection so as to surround the source region. And the foregoing solid-state imaging device is characterized by its capability of reading out the optical signal even without connecting any active loads such as a constant current source to the source which is the output end of the pixel 101. In this event, since a gate potential is maintained constant by an external power source, the surface potential is uniquely decided by the photo-generated holes stored in the heavily doped buried layer. As a state of the photo-generated holes stored in the heavily doped buried layer is not influenced by a source potential, no unnecessary feedback operations are applied on the heavily doped buried layer even if the source potential is changed during the signal reading. Therefore, the surface potential can be accurately transmitted to the source even if the load of the source follower is only a capacitor capable of being readily matched to each other for characteristics, not a constant current source in which it is difficult to match to each other for characteristics. With this, it is possible to read out a signal while suppressing a fixed pattern noise.

According to another present invention, the difference signal generation circuit is provided, as shown in Fig.7 as an example, with a pixel mixing switch device SM which makes connection/disconnection of the amplifiers 105a, 105b of at least two columns, more in detail of the negative input terminals of the operational amplifiers 31 thereof. This structure is adequate to the solid-state imaging device which treats moving image.

Further, the thinning operation can be performed with the above structure by connecting the pixel mixing switch device SM to mix signals from pixels of at least two columns and average them.

Thus, even if thinning is carried out during scanning, since an averaged signal is outputted as a signal in the position of the pixel 101 thinned during scanning, deterioration of MTF can be prevented. Further, since no reduction occurs in a sampling frequency, it is possible to prevent generation of the folding noises and obtain a fine image. Moreover, since the number of times of signal processing is reduced according to the thinning, it is possible to prevent the power consumption from increasing.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a view showing a circuit constitution of a solid-state imaging device of a conventional example.

Fig. 2 is a circuit diagram showing a variable gain

amplifier according to a first embodiment of the present invention.

Fig. 3 is a view showing a circuit constitution of a solid-state imaging device including the variable gain amplifier according to the first embodiment of the present invention.

Figs. 4A and 4B are views showing operations of a signal processing circuit (column type ADC) included in the circuit constitution of the solid-state imaging device of Fig. 3.

Fig. 5 is a timing chart when the solid-state imaging device according to the first embodiment of the present invention is operated.

Fig. 6 is a timing chart showing a difference signal generating operation of the solid-state imaging device according to the first embodiment of the present invention.

Fig. 7 is a view showing a circuit constitution of a solid-state imaging device comprising a signal output circuit according to a second embodiment of the present invention.

Fig. 8 is a timing chart of a pixel mixing operation of the solid-state imaging device according to the second embodiment of the present invention.

Fig. 9 is a plan view showing a device structure in a pixel of an optical sensor array constituting the solid-state imaging device according to each of the first

and second embodiments.

Fig. 10 is a sectional view taken along line I-I of Fig. 9.

5 DESCRIPTION OF THE PREFERRED EMBODIMENTS

Next, description will be made for embodiments of the present invention with reference to the accompanying drawings.

(First Embodiment)

10 (i) Constitution of variable gain amplifier

By referring to Fig. 2, description is made for a specific constitution of a variable gain amplifier 105a which is a first embodiment of the present invention. This variable gain amplifier 105a is an amplifier circuit capable of generating a difference signal between two signals, and is especially characterized by its capability of changing an amplification factor according to an input level of the difference signal.

As shown in Fig. 2, the variable gain amplifier 105a comprises an operational amplifier 31 which includes a positive input terminal (+), a negative input terminal (-), and an output terminal. A reference voltage (Vref) is inputted to the positive input terminal (+) while, for example, a first signal voltage Vt and a second signal voltage Vn which are outputs of a photoelectric conversion device 101 of an optical sensor array 100 are inputted to the negative input terminal (-). From the

output terminal, a difference signal $V_s (=V_t - V_n)$ obtained by subtracting the second signal voltage V_n from the first signal voltage V_t is outputted.

In addition, switch devices SW1 and SW2, and an input capacitor C_i composed of a capacitor C_1 are connected in series in a signal path extending from an input terminal of the variable gain amplifier 105a to the negative input terminal of the operational amplifier 31. One end of the input capacitor C_i is connected through the switch devices SW1 and SW2 to the input terminal of the variable gain amplifier 105a, and the other end thereof is connected to the negative input terminal of the operational amplifier 31. The switch devices SW1 and SW2 are defined as a first switch device.

The switch device SW1 is composed of a single n channel MOS transistor, while the switch device W2 is composed of a transmission gate including one or more MOS transistors. Both of the switch devices turn ON/OFF the signal path to input an input signal to one end of the input capacitor C_i . An output end of the photoelectric conversion device 101, for example, is connected to the input terminal of the variable gain amplifier 105a. In case where a large positive voltage is applied through the output end in order to initialize the photoelectric conversion device 101, the switch device SW1 of the first switch device effectively functions to prevent a high voltage from being inputted to the variable gain

amplifier 105a.

To one end of the input capacitor C1, the reference voltage (Vref) is connected via a switch device (second switch device) SW3. Between the negative input terminal (-) and output terminal of the operational amplifier 31, a feedback capacitor Cf and a switch device (third switch device) SW4 are connected parallel to each other.

The feedback capacitor Cf is composed of a plurality of capacitors C2, C3 and C4. In addition, in order to enable adjustment of a capacitance of the feedback capacitor Cf by optionally selecting the capacitors C3 and C4 among those capacitors C2 to C4, fifth and sixth switch devices SW5 and SW6 are provided to connect/disconnect the respective capacitors C3 and C4 between the negative input terminal (-) and the output terminal of the operational amplifier 31.

Note that the feedback capacitor Cf may be composed of three or more capacitors which can be selectively connected/disconnected between the negative input terminal (-) and the output terminal of the operational amplifier 31 in addition to the capacitor C2 whose connection is fixed, and three or more corresponding switch devices SW5, SW6, . . . may be provided to connect/disconnect the respective capacitors C3, C4, . . .

The output terminal of the operational amplifier 31 is connected to an input of a column type ADC 106 for each column. In this event, if a difference signal

outputted from the operational amplifier 31 is out of a range of a digital encoding analog input level to the column type ADC 106 of a next stage, an amplifying gain needs to be adjusted to set the difference signal within the range of the analog input level. Accordingly, signals (Gsel1 and Gsel2) are supplied manually or automatically from the outside in order to select at least one of the fifth and sixth switch devices SW5 and SW6 to control ON/OFF thereof. In other words, the adjustment of the amplifying gain of the operational amplifier 31 can be performed by adjusting a ratio (C_i/C_f) of the input capacitor C_i with respect to the feedback capacitor C_f connected between the negative input terminal (-) and the output terminal of the operational amplifier 31. In the embodiment, the feedback capacitor C_f is composed of the plurality of capacitors C2 to C4, and is constituted as capable of optionally selecting a proper capacitor by turning ON/OFF the switch device SW5 or SW6.

Note that although the foregoing switch devices SW1 to SW6 are schematically shown in the drawing, the same function can be achieved in practice by using one or more transistors, similarly to the case of the above-described switch devices SW1 and SW2.

(ii) Constitution of solid-state imaging device

Next, description is made for a solid-state imaging device to which the variable gain amplifier 105a of Fig.

2 is applied.

Fig. 3 is a view showing a circuit constitution of the solid-state imaging device according to the first embodiment of the present invention. As shown in Fig. 3, this solid-state imaging device is provided with an optical sensor array 100 and a signal output circuit 107. The signal output circuit 107 is provided with a difference signal generation circuit 105 each column disposing the variable gain amplifier 105a of Fig. 2 and a column type analog/digital converter (referred to as a column type ADC, hereinafter) 106. By driving MOS transistors of pixels (photoelectric conversion devices) 101 arrayed in rows, the signal output circuit 107 outputs, for respective rows, digitized video signals (Vout1,... Voutn) which is proportional to a quantity of incident light and containing no second signal voltage Vn components.

First, the optical sensor array 100 is described. This optical sensor array 100 employs a two-dimensional constitution where the pixels 101 are arrayed in a matrix form of rows and columns.

Next, a device structure in each of the pixels 101 is described. Fig. 9 is a plan view showing a device layout in the pixel 101; and Fig. 10 is a sectional view showing a device sectional structure in the pixel, which corresponds to a sectional view taken along line I-I of Fig. 9.

The pixel 101 includes a photo diode 111 and a MOS transistor 112 for detecting an optical signal, which are provided adjacently to each other.

The photo diode 111 and the MOS transistor 112 are respectively formed in different well regions, i.e., a first well region 15a and a second well region 15b which are connected to each other. The first well region 15a having the photo diode 111 formed therein constitutes a part of a region where charges are generated by light irradiation. The second well region 15b having the MOS transistor 112 formed therein is defined as a gate region where a channel threshold voltage can be changed by a potential applied to the region 15b.

A drain region 17a of the MOS transistor 112 is formed so as to surround an outer peripheral part of a ring-shaped gate electrode 19, and a source region 16 is formed so as to be surrounded by an inner periphery of the ring-shaped gate electrode 19.

The drain region 17a is extended to form an impurity region 17 of the photo diode 111. That is, the impurity region 17 and the low-concentration drain region 17a are formed as one body such that most parts of the regions are placed on surface layers of the first and second well regions 15a and 15b connected with each other.

In addition, a carrier pocket (heavily doped buried layer) 25 which is a feature of the solid-state imaging device is formed in a peripheral part of the source

region 16 so as to surround the same in the second well region 15b below the gate electrode 19.

5 The drain region 17a is connected through a contact region 17b to a drain voltage (VDD) supply line (or drain electrode) 22; the gate electrode 19 is connected to a vertical scanning signal (VSCAN) supply line 21; and the source region 16 is connected to a vertical output line (or source electrode) 20.

10 The foregoing constituent components of the pixel 101 are covered with a light transmissive insulating film, and a region other than that of a light-receiving window 24 of the photo diode 111 is shielded from a light by a metal layer (light shielding film) 23 formed on the insulating film.

15 Next, description is made for a peripheral circuit for driving the pixels 101 arrayed in the rows and columns by referring to Figs. 2, 3, 9 and 10. Though not shown in the drawings, a driving scanning circuit of a vertical scanning signal (VSCAN) and a driving scanning
20 circuit of a drain voltage (VDD) are disposed around the pixel 101 to supply signals for scanning the pixel 101.

25 From the driving scanning circuit of the vertical scanning signal (VSCAN), the vertical scanning signal supply line 21 comes out for each row. Each vertical scanning signal supply line 21 is connected to the gate electrode 19 of the MOS transistor 112 in each of all the pixels 101 arrayed in the row direction.

From the driving scanning circuit of the drain voltage (VDD), the drain voltage supply line (VDD supply line) 22 comes out for each row. Each drain voltage supply line (VDD supply line) 22 is connected to the drain region 17a of the MOS transistor 112 in each of all the pixels 101 arrayed in the row direction.

Vertical output lines 20a and 20b are provided for respective columns. These vertical output lines 20a and 20b are respectively connected to the source region 16 of the MOS transistor 112 in each of all the pixels 101 arrayed in the column direction. A booster circuit, not shown, is connected to each of the vertical output lines 20a and 20b to supply a large positive voltage for initialization of the pixel 101. In other words, a boosted voltage is applied to the source region 16 of the MOS transistor 112 of each pixel 101 for each column. The boosted voltage is passed on through a capacitor between the gate and source of the MOS transistor 112, and is lastly applied to the gate region 19. Thus, carrier sweeping can be promoted by increasing electric field strength applied to the well regions 15a and 15b.

The source region 16 of the MOS transistor 112 is connected through the vertical output lines 20a and 20b to an input end of the signal output circuit 107. In other words, the source region 16 is connected to the input end of the difference signal generation circuit 105 in the signal output circuit 107 for each column, and is

directly connected to the input capacitor C_i shown in Fig. 2 when a signal is read out. Though omitted in Fig. 3, on midways of the vertical output lines 20a and 20b, switch devices are provided, in practice, to control signal flows.

A first signal voltage V_t and a second signal voltage V_n are inputted to the input end of the difference signal generation circuit 105. From the output terminal of the difference signal generation circuit 105, there is outputted a difference signal V_s ($=V_t - V_n$) which is obtained by subtracting the second signal voltage V_n generated upon initialization of the pixel 101 from the first signal voltage V_t . Moreover, the output of the difference signal generation circuit 105 is connected to the input end of the column type ADC 106 for each column.

In the difference signal generation circuit 105, by selecting a capacitance of the feedback capacitor C_f based on the signals G_{sel1} and G_{sel2} from the outside, gain adjustment can be performed in such a way as to set the level of the difference signal V_s within the range of the digital encoding analog input level. Thus, by performing gain adjustment when necessary, the difference signal V_s or V_{samp} which has an output level adjusted is outputted from the output terminal.

The column type ADC 106 compares the difference signal V_s or V_{samp} as an analog signal with a comparison

lamp voltage VL having a predetermined gradient by a not-shown comparator as shown in Figs. 4A and 4B, and converts the difference signal Vs or Vsamp into a pulse count Nc or Nca corresponding to the amplitude of the difference signal Vs or Vsamp by use of a not-shown pulse counter. Note that the pulse count Nca is multiplied by a coefficient in consideration of an amplifying gain, and is thereby converted into the pulse count Nc corresponding to the actual difference signal Vs.

A digitized video signal is outputted from the output terminal of the column type ADC 106 while corresponding to a pixel array of each row.

As described above, according to the solid-state imaging device of the embodiment of the present invention, the difference signal corresponding to the optical signal can be amplified by a gain so as to set the difference signal in the range of the digital encoding analog input level.

In addition, the foregoing solid-state imaging device is characterized by its capability of reading out the optical signal even without connecting any active loads such as a constant current source to the source region 16 which is the output end of the pixel 101. This is attributed to the fact that the MOS transistor 112 for signal detection includes the heavily doped buried layer 25 for storing photo-generated charges (holes), which is provided below the channel so as to surround the source

region 16. The reason for the above is as follows.

Photo-generated holes are stored in a potential well of the p-type heavily doped buried layer 25, and thus a threshold voltage is modulated by changing an amount of negative space charges in the depleted well region 15b. Thus, a surface potential of the MOS transistor 112 is decided. In this event, since a gate potential is maintained constant by an external power source, the surface potential is uniquely decided by the photo-generated holes stored in the potential well. As a state of the photo-generated holes stored in the heavily doped buried layer 25 is not influenced by a source potential, when a source follower having a signal charge storage capacitor as a load is formed to read out a signal, no unnecessary feedback operations are applied on the heavily doped buried layer 25 even if the source potential is changed during the signal reading. Accordingly, it is not necessary to maintain a potential difference between the source and the gate constant by connecting the constant current source to the source region 16 of the MOS transistor 112. Thus, the surface potential can be accurately transmitted to the source even if only capacitors capable of being readily matched for characteristics are set as the load of the source follower.

Therefore, it is possible to read out a signal while suppressing a fixed pattern noise.

(iv) Detecting and reading operations of optical signal

Next, description is made for optical signal detecting and reading operations of the first embodiment
5 of the present invention by referring to Figs. 4 to 6.

Each of Figs. 4A and 4B shows an operation of the column type ADC 106.

Fig. 5 is a timing chart illustrating optical signal detecting and reading operations by focusing on the pixel
10 101, where the foregoing MOS transistor for optical signal detection is an nMOS transistor.

Fig. 6 is a timing chart for an operation of the difference signal generation circuit 105, where Vout1, ...
15 Voutn denote digitized video signals outputted from the signal output circuit 107.

In the optical signal detecting and reading operations, as shown in Fig. 5, a series of steps including a storing period, a signal reading period, a sweeping period (initializing period), and a noise
20 reading period are repeated.

First, the series of steps are described by referring to Fig. 5. For convenience, the description is started from the storing period. When necessary, reference may also be made to Figs. 2, 3, 9 and 10.

25 In the storing period, the photo diode 111 is irradiated with a light to generate photo-generated holes. These photo-generated holes are transferred below the

channel region of the MOS transistor 112, and stored in the heavily doped buried layer 25. Accordingly, since a threshold voltage of the MOS transistor 112 is changed, in the next reading period, the change of the threshold voltage is outputted as a source voltage V_{ps} .

In the signal reading period, the MOS transistor 112 is operated to output the source voltage V_{ps} as an optical signal proportional to a storage quantity of photo-generated holes, and the source voltage V_{ps} is stored in the input capacitor C_i . The source voltage V_{ps} constitutes a signal voltage V_t obtained by converting the optical signal into the electric signal, and contains a second signal voltage component V_n in addition to a pure signal voltage component V_s according to light intensity.

In the initializing period, the switch device SW_1 is disconnected, high voltages are applied through the source region 16 of the MOS transistor 112 to the gate electrode 19 and the drain region 17a, and the stored holes are discharged from the photo diode 111 and the MOS transistor 112 for optical signal detection, thereby initializing the pixel 101.

In the noise reading period, the source voltage V_{ps} in the initialized state is outputted as the second signal voltage V_n from the pixel 101, and then inputted to the signal output circuit 107 to output a difference signal $V_s (=V_t - V_n)$ obtained by removing the second signal

voltage V_n .

After the end of the noise reading period, the process returns to the foregoing storing period again.

Next, by referring to Fig. 6, detailed description
5 is made for an operation for generating a digitized difference signal V_s while corresponding to the series of steps including the storing period, the signal reading period, the sweeping period (initializing period), and the noise reading period by focusing on the variable gain
10 amplifier 105a (in the difference signal generation circuit 105) of Fig. 2.

In the storing period, signals SCM and CLM are both set to high levels (referred to as H levels, hereinafter), and the switch devices SW2 and SW4 are connected.
15 Signals Load and RSM are both set to low levels (referred to as L levels, hereinafter), and the switch devices SW1 and SW3 are disconnected.

In a period (input capacitor initializing period) at the end of the storing period, the signals Load, SCM, RSM, CLM, Gsel 1, and Gsel 2 are all set to H levels to turn
20 ON (connect) the switch devices SW1 to SW6, and then charges of the capacitor C1 as the input capacitor C_i and of the capacitors C2 to C4 as the feedback capacitor C_f are initialized.

25 Then, in the sensor signal reading period (signal reading period), the signal RSM is set to the L level to turn OFF (disconnect) the switch device SW3. The other

switch devices SW1, SW2 and SW4 are maintained in the previous states thereof. Accordingly, a first signal voltage V_t from each pixel 101 is supplied to the input capacitor C_i of the difference signal generation circuit 105. However, this signal voltage V_t contains an optical signal component V_s and a second signal voltage component V_n at the initialization of the pixel 101.

In this event, a potential difference between both ends of the input capacitor C_i of the difference signal generation circuit 105 is set to $V_t - V_{ref}$. Then, since the switch device SW4 is ON, an output of the operational amplifier 31 of the difference signal generation circuit 105 becomes V_{ref} .

In the pixel initializing period (initializing period), the signals Load and SCM are set to L levels to turn OFF the switch devices SW1 and SW2. The other switch devices SW3 and SW4 are maintained in the previous states thereof. Meanwhile, a high voltage is applied to the output end of the pixel 101 to initialize the pixel. That is, the stored charges are removed from the photo diode 111 and the MOS transistor 112.

Thereafter, in the noise reading period, in a period of rising (signal line initializing period), the vertical output lines 20a and 20b are set to ground potentials through a not-shown switch device, the signal SCM is set to the L level, and the switch device SW2 is maintained in disconnection. Furthermore, while setting the signal

CLM to the L level to disconnect the switch device SW4, the signal Gsell is set to the H level to connect the switch device SW5 and thus select the capacitor C3, and the feedback capacitor Cf is set as equal to the input capacitor Ci. Here, a capacitance equal to the capacitance of the input capacitor Ci is set to C2+C3. Furthermore, the signals Load and RSM are set to the H level to connect the switch devices SW1 and SW3. Thus, charges stored in the signal line including the input capacitor Ci in the difference signal generation circuit 105 are initialized. In addition, since one end side of the input capacitor Ci becomes Vref, the charges $C_i \cdot (V_t - V_{ref})$ stored in the input capacitor Ci are transferred to the feedback capacitor Cf ($=C_2+C_3$). Thus, a potential difference between both ends of the input capacitor Ci becomes zero.

After the passage of the signal line initializing period, while setting the signal SCM to the H level to connect the switch SW2, the signals RSM and CLM are set to the L level to disconnect the switches SW3 and SW4. Moreover, the signal Gsell is set to the H level to connect the switch SW5 and thus select the capacitor C3. Thus, the potential difference between both ends of the input capacitor Ci of the difference signal generation circuit 105 is changed from zero to $V_n - V_{ref}$. A charge $C_i \cdot (V_t - V_n) / C_f (=V_s)$ corresponding to the above is also stored in the feedback capacitor Cf, and an output of the

operational amplifier 31 becomes a signal voltage ($V_{ref}-V_s$) containing the difference signal V_s .

Then, the difference signal V_s is compared with the range of the digital encoding analog input level. If a level of the difference signal V_s is within the range of the digital encoding analog input level, the difference signal is directly outputted to the column type ADC 106.

On the other hand, when the level of the difference signal V_s is smaller than, for example a lower limit of the range of the digital encoding analog input level, a capacitance of the feedback capacitor C_f is selected based on a signal from outside such that the difference signal V_s is amplified by a gain so as to set the level of the difference signal V_s larger than the lower limit. Here, if a capacitance capable of obtaining a necessary amplifying gain is $C_2+C_4(<C_2+C_3)$, the signal $G_{sel} 1$ is set to the L level to disconnect the switch SW_5 , the signal $G_{sel} 2$ is set to the H level to connect the switch SW_6 , and the capacitor C_2+C_4 is selected as the feedback capacitor C_f .

Then, after the initialization of the input capacitor C_i and the feedback capacitor C_f , a new first signal voltage V_t and a new second signal voltage V_n are sequentially inputted to the input capacitor C_i to be converted into charges, and the charges are then transferred to the feedback capacitor C_f . Sequentially, a new second signal voltage V_n is inputted to the input

capacitor C_1 to be converted into charges, and the charges are then transferred to the feedback capacitor C_f . In other words, the potential difference between both sides of the capacitor C_1 of the input capacitor C_i is changed from $V_t - V_{ref}$ to $V_n - V_{ref}$ via zero. A charge $C_i \cdot (V_t - V_n) / C_f (= V_{samp})$ corresponding to the above is also stored in the capacitor ($C_2 + C_4$) as the feedback capacitor C_f , and a signal voltage ($V_{ref} - V_{samp}$) containing a difference signal V_{samp} amplified is outputted from the output of the operational amplifier 31.

Then, the difference signal V_s or V_{samp} is inputted to the column type ADC 106 shown in Fig. 2 and is converted into a digital signal. Furthermore, this digital signal is outputted as a video signal from the output terminal of the column type ADC 106.

Besides, the amplifier which has an offset value is provided each column. Therefore, it is supposed that an output signal of the column type ADC 106 includes the offset component each column. This offset component can be readily removed by the following way. It is the way of converting the offset to a digital signal and memorizing it, followed by adding it as a signal for compensation at the detection of an optical black signal during a blanking period, and then digitally operating to remove the digital optical black signal from the digital difference signal.

The present invention has been described above in

detail according to the first embodiment. However, a scope of the present invention is not limited to the example specifically described in the foregoing embodiment, and changes and modifications of the foregoing embodiment without departing from the teachings of the present invention are within the scope of the present invention.

For example, as a reference for comparing the difference signal, the range of the digital encoding analog input level is used. However, there is no limitation in this regard.

(Second Embodiment)

(i) Constitution of solid-state imaging device

By referring to Fig. 7, description is made for a constitution of a solid-state imaging device according to a second embodiment of the present invention. Fig. 7 is a view showing a circuit constitution of the solid-state imaging device according to the second embodiment of the present invention.

In this solid-state imaging device, this embodiment is different from the first embodiment, as shown in Fig. 7, in that a switch device (a pixel mixing switch device) SM is provided between a negative input terminal (-) of an operational amplifier 31 of a variable gain amplifier 105a of one column and a negative input terminal (-) of an operational amplifier 31 of a variable gain amplifier 105b of adjacent column thereto among variable gain

amplifiers 105a, 105b, . . which each is provided each column in a difference signal generation circuit 105.

5 The arrangement of an optical sensor array 100 according to this embodiment is correspondent with a basic color filter array of Bayer system. In this color filter array, "R", "G", "B" pixels are arranged in four regions adjacent to each other, and "G" pixels of same color are arranged obliquely to each other. Vertical output lines 20a, 20b connected to the "G" pixels are
10 connected to the input ends of the variable gain amplifiers 105a, 105b, respectively.

This circuit construction corresponds to the same one as the first embodiment by disconnecting the switch device SM, and thus the circuit can be driven similar to
15 the first embodiment. On the other hand, the difference signals of the "G" pixels of at least two columns adjacent to each other are mixed by connecting the switch device SM applying a switching signal MODE, and thus averaged video signals can be outputted from the
20 respective column output ends of the circuit.

Besides, the variable gain amplifiers 105a, 105b . . are applied as an amplifier for a signal voltage outputted from a pixel. However, the amplifiers in which the capacitors C3, C4 and switch devices SW5, SW6 are
25 omitted from the variable gain amplifiers 105a, 105b . . may be used if gain adjustments are not necessary.

(ii) Photodetecting operation

Next, by referring to drawings, description is made for a photodetecting operation of the solid-state imaging device according to the second embodiment.

The solid-state imaging device according to this embodiment is capable of performing both the ordinary operation similar to the first embodiment and a pixel mixing in the thinning operation. For the ordinary operation, the switch device SM is disconnected to correspond to the same circuit construction as the first embodiment, and thus the circuit is operated similarly to the first embodiment. With this, a level-adjusted video signal can be outputted.

Next, a thinning operation is described as follows. Fig. 8 is a timing chart for a thinning operation performed by using the difference signal generation circuit 105 of Fig. 7. The description necessarily refers to Fig. 7. In this case, the feedback capacitor Cf is assumed to be composed of only C2 among the capacitors C2, C3, C4.

In the optical signal reading operation including the pixel mixing operation of this embodiment, a series of steps including a storing operation, a signal reading operation, a sweeping operation (initializing operation), and a noise reading operation are repeated. The pixel mixing operation is performed simultaneously during the noise reading operation.

First of all, from the storing operation to the

initializing operation of a signal line, the pixel-mixing switch device SM is disconnected to perform the same operation as that being described in Fig.6 of the first embodiment. Accordingly, charges $C_i \cdot (V_{ta} - V_{ref})$ is accumulated in the feedback capacitor C_f of the variable gain amplifier 105a, and charges $C_i \cdot (V_{tb} - V_{ref})$ is accumulated in the feedback capacitor C_f of the variable gain amplifier 105b while the signal line including the input capacitor C_i is initialized.

Sequentially, the operation is shifted to the noise reading operation. During the noise reading operation, the signal MODE is set to H level to connect the switch device SM. Thus, the negative input terminals of the operational amplifiers 31 of the variable gain amplifiers 105a, 105b of the adjacent two columns are connected to each other. The connection results in the state of capable of performing a pixel mixing. Simultaneously, the signal SCM is set to H level to connect the switch device SW2, and the signal RSM is set to L level to disconnect the switch device SW3 while the switch device SW1 is maintained in connection and the switch device SW4 is maintained in disconnection. Those result in the state of capable of inputting the second signal voltage V_{na} , V_{nb} from the pixels 101.

In the variable gain amplifier 105a, an input of the second signal voltage V_{na} from the pixel 101 is

expected to allow the potential difference between the
 both ends of capacitor C1 to change from 0 to $V_{na}-V_{ref}$
 and to allow the potential difference between the both
 ends of capacitor C2 to change to $C1 \cdot (V_{ta}-V_{na})/C2$. And
 5 in the variable gain amplifier 105b, an input of the
 second signal voltage V_{nb} from the pixel 101 is
 expected to allow the potential difference between the
 both ends of capacitor C1 to change from 0 to $V_{nb}-V_{ref}$
 and to allow the potential difference between the both
 10 ends of capacitor C2 to change to $C1 \cdot (V_{tb}-V_{nb})/C2$. In
 this case, since the input ends of the capacitors C2 of
 the variable gain amplifiers 105a, 105b are connected
 to each other, charges which should be separately
 accumulated in respective capacitors C2 are mixed and
 15 averaged. The potential difference ΔV_0 between the
 both ends of each capacitor C2 results in approximately
 $C1/C2 \cdot ((V_{ta}-V_{na})+(V_{tb}-V_{nb}))/2$. Further, the output of
 the each operational amplifier 31 results in $V_{ref}-\Delta V_0$.
 Afterwards, the signals are suitably processed to
 20 output the video signal of "G" from the video signal
 output terminal.

Incidentally, in the conventional typical solid-
 state imaging device, because of thinning of sampling
 pixels, MTF is deteriorated, an image of much moire is
 25 formed, or folding noises are generated. In addition,
 since the image sensor needs to be operated at a high
 speed, power consumption is increased.

On the other hand, according to the embodiment, by connecting the switch device SM, signals outputted from pixels 101 of at least two columns are mixed and averaged, thereby generating video signal regarding the thinning.

5 Thus, even if thinning is carried out, deterioration of MTF is prevented. Since averaged video signals in the position of the pixel 101 thinned during scanning is outputted, no reduction occurs in a sampling frequency. As a result of the above, it is possible to prevent
10 generation of the folding noises.

Moreover, since the number of times of signal processing is reduced according to the thinning, it is possible to prevent the increase in the power consumption. Further, multi-function of the signal output circuit is
15 attained with a simple means of the switch device SM.

The present invention has been described above in detail according to the second embodiment. However, a scope of the present invention is not limited to the example specifically described in the foregoing
20 embodiment, and changes and modifications of the foregoing embodiment without departing from the teachings of the present invention are contained within the scope of the present invention.

For example, in the second embodiment, though there
25 is applied the basic color filter array of the Bayer system as the color array, the color filter array of the other system may be applied.

Further, various modified examples may be used as the photoelectric conversion device applied to the solid-state imaging device according to this invention. This is the same in the first embodiment as well. In those
5 embodiment, there is used the photoelectric conversion device having the same structure as that of a photoelectric conversion device described in Japanese Patent (Patent Registration No. 2935492). However, there may be used photoelectric conversion devices of other
10 structures such that an accurate signal voltage can be obtained even if a capacitor is directly connected to an output thereof.

Furthermore, the first and second well regions 15a and 15b are formed in the n-type epitaxial layer 12 on
15 the p-type substrate 11. However, instead of the n-type epitaxial layer 12, a p-type epitaxial layer may be used. In this case, n-type impurities may be introduced into the p-type epitaxial layer to form an n-type well layer, and then first and second well regions 15a and 15b may be
20 formed in the n-type well layer.

As described above, according to the present invention, even when amplitude of the analog difference signal is smaller than the suitable range of the digital encoding analog input level, the analog difference signal
25 can be amplified to be suitably set within the requested range of the digital encoding analog input level.

As a result, when the analog difference signal is

digitized, it is possible to secure the dynamic range and to improve the S/N ratio.

Moreover, the foregoing solid-state imaging device is characterized by including the heavily doped buried layer for storing photo-generated charges, which is provided below the channel of the MOS transistor for signal detection so as to surround the source region. And the foregoing solid-state imaging device is characterized by reading out the optical signal with directly connecting the source of the output of the pixel to only capacitor capable of being readily matched to each other for characteristics, without connecting it to a constant current source in which it is difficult to be matched to each other for characteristics. Therefore, the surface potential can be accurately transmitted to the source, and thus it is possible to read out a signal while suppressing a fixed pattern noise.

Furthermore, according to the other present invention, the pixels are arrayed in rows and columns, the amplifier is provided for each column to process an output signal from each pixel, and the pixel-mixing switch device is provided between the input terminals of the operational amplifiers in the amplifiers of at least two columns. During thinning, the switch device is connected, so that signals from pixels of at least two columns are mixed to be averaged and is outputted as a video signal of each pixel. Thus, it is possible to

obtain an image with no folding noise, i.e., an image with no moire, and to reduce the power consumption.